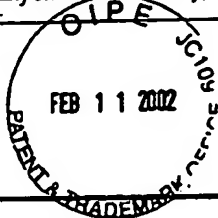


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	Filing Date: December 5, 2001	



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		4,661,901		Veneski	4-28-87	
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		EP	0415542 A1	A1	Advanced Micro Devices, Inc.	03/06/91		
		EP	0630115 A2	A2	Pilkington Micro-Electronics Limited	12/21/94		
		GB	2180382 A		Pilkington Micro-Electronics Limited	03/25/87		
		GB	2295738 A		Altera Corporation	06/05/96		

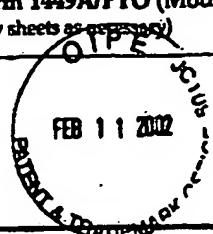
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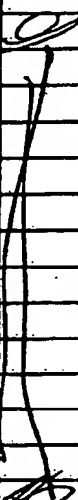
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		5,243,238		Kean	9-7-93	
		5,260,610		Pedersen et al.	11-9-93	
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		5,298,805		Garverick et al.	3-29-94	
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		PCP	WO92/08286	A1	Concurrent Logic, Inc.	05/14/92		
		BET (28)	WO94/28475	A1	Regents of the University of California	12/08/94		
		BGT (28)	WO96/05964	A1	Minnesota Mining and Manufacturing Company	02/29/96		
		BCT (28)	WO96/35261	A1	BTR, Inc.	11/07/96		

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		WO	94/10754	A1	Xilinx, Inc.	05/11/94		
		WO	95/04404	A1	Advantage Logic, Inc.	02/09/95		

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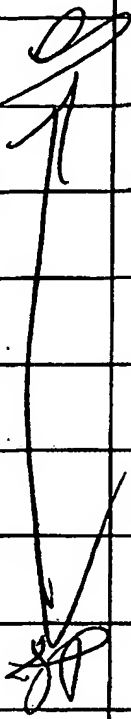
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		Filing Date: December 5, 2001	
OTHER ART - NO PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
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		DAVE BURSKY, "Fine-Grain FPGA Architecture Uses Four Levels of Configuration Hierarchy", Electronic Design, pp. 33-34, October 1, 1993.	
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